CLAIMS

I/We Claim:

1. A method for providing a bus, the bus having associated time periods for transferring a number D data bits during each time period, comprising:

receiving the D data bits and a clock bit;

mapping the D data bits and the clock bit onto a number B bus lines to produce mapped data bits and one mapped clock bit, the number B being equal to D plus at least one, wherein the clock bit is mapped onto at least one bus line, the at least one bus line also being used by at least one data bit at a different time period; and

transmitting the mapped data bits and one mapped clock bit on the bus.

2. The method of claim 1, wherein D equals nine.

3. The method of claim 1, wherein D equals eight.

4. The method of claim 1, wherein D is less than eight.

5. The method of claim 1, wherein D is greater than nine.

6. The method of claim 1, wherein the data bits are encoded before the step of mapping.

7. The method of claim 1 wherein the one mapped clock bit produces positive-edge signals.

8. The method of claim 1 wherein the one mapped clock bit produces negative-edge signals.

9. A method for providing information on a bus, the bus having associated time periods for transferring a number D data bits during each time period, comprising:

receiving the D data bits and at least one clock bit;

mapping the D data bits and the clock bit onto a number B bus lines to produce mapped data bits and a mapped clock bit set, the number B being less than or equal to D plus one, wherein the mapped clock bit set is mapped onto a corresponding number of different bus lines at some different time periods; and

transmitting the mapped data bits and the mapped clock bit set on the bus.

10. The method of claim 9, wherein the mapped clock bit set is mapped to a single bus line.

11. The method of claim 9, wherein the mapped clock bit set is mapped to a plurality of bus lines.

12. The method of claim 9, wherein D equals nine.

13. The method of claim 9, wherein D equals eight.

14. The method of claim 9, wherein D is less than eight.

15. The method of claim 9, wherein D is greater than nine.

16. The method of claim 9, wherein the data bits are encoded before the step of mapping.

17. The method of claim 9 wherein the one mapped clock bit produces positive-edge signals.

18. The method of claim 9 wherein the one mapped clock bit produces negative-edge signals.

19. A method for providing a bus, the bus having associated time periods for transferring a number D data bits during each time period, comprising:

receiving the data bits and at least one clock bit;

mapping the data bits and clock bit onto a number of bus lines, wherein the data bits and clock bit are not mapped to the number of bus lines identically in at least some successive time periods.

20. A method for providing a bus, the bus having associated time periods for transferring a number D data bits during each time period, comprising:

receiving the data bits and at least one clock bit from the bus;

demapping the data bits and the at least one clock bit, wherein data bits and the at least one clock bit are not demapped identically in at least some successive time periods.

21. An integrated circuit, comprising:

a bus, the bus having associated time periods for transferring a number D data bits during each time period;

a multiplexer having inputs capable of receiving D data bits and a clock bit, the multiplexer mapping the data bits and clock bit onto a corresponding number of different bus lines at some different time periods.

22. A computing device, comprising:

a bus, the bus having associated time periods for transferring a number D data bits during each time period;

a multiplexer having inputs capable of receiving the D data bits and a clock bit, the multiplexer mapping the data bits and clock bit onto a

corresponding number of different bus lines at some different time periods.

23. A method for providing a bus, the bus having associated time periods for transferring a number D data bits during each time period, comprising:

receiving the D data bits and a clock bit;

mapping the D data bits and the clock bit onto a number B bus lines to produce mapped data bits and at least one mapped clock bit, the number B being equal to D plus at least one, wherein the at least one clock bit is mapped onto at least one bus line such that the at least one clock bit is mapped over multiple time periods onto the bus lines in a cyclic manner; and

transmitting the mapped data bits and one mapped clock bit on the bus.

24. The method of claim 23, wherein D equals nine.

25. The method of claim 23, wherein D equals eight.

26. The method of claim 23, wherein D is less than eight.

27. The method of claim 23, wherein D is greater than nine.

28. The method of claim 23, wherein the data bits are encoded before the step of mapping.

29. The method of claim 23 wherein the one mapped clock bit produces positive-edge signals.

30. The method of claim 23 wherein the one mapped clock bit produces negative-edge signals.